REMARKS

The Examiner is thanked for the continued indication that claims 3 and 14 define allowable subject matter. The Office Action, however, has continued to reject all remaining claims.

Discussion of Rejections Under 35 U.S.C. § 112, First Paragraph

The Office Action rejected all claims under 35 U.S.C. § 112, first paragraph. In this regard, the Examiner stated that the claimed subject matter was not supported by the specification, and that the previous amendments to claims 1, 11, and 20 were not supported by the specification. Applicant respectfully disagrees. In this regard, Applicant respectfully submits that the features introduced into the claims by the previous amendments embody a fundamental aspect of embodiments described throughout the specification. In the regard, by way of example, claim 1 was previously amended as annotated below:

> 1. An integrated circuit component comprising:
>
> logic capable of being configured to interface with a first portion of a system bus, wherein the first portion of the system bus comprises a first plurality of signal lines of the system bus, but not all of the signal lines of the system bus; and
>
> logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus, wherein the second portion of the signal bus comprises a second plurality of signal lines of the system bus, which are not a part of the first plurality of signal lines.

This amendment is clearly supported by the specification, including, for example, paragraph 0018 (beginning on page 6, line 7) which states:

> As illustrated in FIG. 1, a conventional configuration includes integrated circuit components 102 and 110 that intercommunicate across a system bus 105. ***In the inventive system 200 of FIG. 2, the system bus 105 is split, so that approximately one half of the bus is directed to integrated circuit component 210, while the remaining portion of the bus 105 is directed to integrated circuit component 211.*** A split bus logic component 214 is provided to interface with the portion of the system bus 105 directed to that particular integrated circuit component. Both integrated circuit components 210 and 211 have blocks denoted by reference numerals 214 and 215. In one embodiment, the circuitry and logic within the split bus logic components 214 and 215 are identical. However, the logic blocks have been denoted with differing reference numerals to indicate a differing functionality, based upon the configuration of those logic blocks. For example, in the configuration illustrated in FIG. 2, the split bus logic blocks 214 are configured to interface with a portion of the system bus 105. Split bus logic blocks 215 are configured to interface with the companion logic block of the companion integrated circuit component. Thus, the split bus logic block 215 of component 210 interfaces directly with the split bus logic block 215 of component 211.

(*Emphasis Added*.) Paragraph 0018, and the language emphasized above clearly supports the previous amendments. Indeed, the very purpose of the "split bus logic" is to accommodate or enable communications between the integrated circuit components and a host through less than all signal lines of the system bus. Accordingly, Applicant submits that the rejection under 35 U.S.C. § 112, first paragraph be withdrawn.

Substantively similar amendments were made to claims 11 and 20, and therefore the rejections of those claims should be withdrawn for the same reason.

Discussion of Rejections Under 35 U.S.C. § 112, Second Paragraph

The Office Action rejected all claims under 35 U.S.C. § 112, second paragraph for various, stated reasons. Applicants respectfully submit that each of these rejections should be withdrawn.

The Office Action rejected claim 20 stating that the language "comprises a plurality of signal of signal lines of the system bus" is unclear. Applicants agree (as this was a clear typo), as have amended claim 20 to delete the duplicative language. The Office Action also stated that the language "collectively, the conductive pins of the integrated circuit component" is unclear. Applicants suggest that the Examiner consider the entire claim phrase, which reads: "collectively, the conductive pins of the integrated circuit component do not directly accommodate all signals lines of the system bus, but rather directly accommodate fewer than all of the signal lines of the system bus." Applicants submit that this language is clear, and do not understand what the examiner finds unclear about the language. As repeatedly described throughout the specification, the integrated circuit components of embodiments of the invention permit a smaller pin count, by directly connecting to only a portion of the system bus. Accordingly, Applicant submits that claim 20, as amended herein is fully compliant with all statutory requirements, including the requirements of 35 U.S.C. § 112, second paragraph.

The Office Action then rejected all claims under 35 U.S.C. § 112, second paragraph, alleging that "essential structure cooperative relationships between elements in the claims … have been omitted." In support of this rejection, the Office Action cites MPEP 2172.01 (Unclaimed Essential Subject Matter), and states that "MPEP 2172.01 requires that relationships between elements recited in claims must be specified." This reflects a misunderstanding of MPEP 2172.01. In fact, MPEP 2172.01 specifically states:

> … *Ex parte Nolden*, 149 U.S.P.Q. 378, 380 (Bd. Pat. App. 1965)("It is not essential to a patentable combination that there be interdependency

> between the elements of the claimed device or that all the elements operate concurrently toward the desired result"); *Ex parte Huber*, 148 U.S.P.Q. 447, 448-449 (Bd. Pat. App. 1965) (A claim does not necessarily fail to comply with 35 U.S.C. 112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.

Thus, MPEP 2172 states just the opposite of what the Office Action appears to allege.

Pursuant to the invitation set out at the top of page 4 of the Office Action (underlined), Applicants hereby note their disagreement with the position taken by the Office Action, and submit that the claims, as filed, recited all necessary or essential interrelationships between the elements. In this regard, Applicants note that each claim element makes appropriate relational reference to other claim elements, such that no element is in isolation and therefore appropriate and proper structural interrelationships among claim elements are properly provided. In addition, the Examiner stated that the claims are indefinite because they allegedly do not recite the required structural interrelationship of "essential elements to the claimed invention." The MPEP, however, does not define what is an "essential" element, nor did the Examiner provide a definition of what constitutes an "essential" element.

On page 13 of the Office Action, the Examiner states: "the word(s) –connected— or –operatively connected— may be used to provide essential structural cooperative relationships between structural elements recited in the claims." As the examiner correctly noted, such term "MAY" be used. However, these terms are not REQUIRED in order for claims to be fully compliant with 35 U.S.C. § 112, second paragraph.

Further, and despite Applicants' invitation in the previous response, the Examiner has still not set forth any detailed explanation or illustration of why the claims allegedly

failed to satisfy MPEP 2172. The Examiner apparently had a good working understanding of the claims (as is required by MPEP 904 before initiating a search, and as reflected in the application of prior art as allegedly anticipating the claims). Accordingly, Applicants respectfully request the Examiner to provide more helpful insight into this rejection, should the Examiner disagree with Applicants' position and maintain this rejection. In reconsidering this rejection, however, Applicants remind the Examiner that claim breadth should not be confused with indefiniteness (see MPEP 2173.04).

In view of the foregoing, Applicants respectfully submit that all claims, as amended, fully comply with the requirements of 35 U.S.C. § 112, second paragraph, and Applicants respectfully request that the rejections thereof be reconsidered and withdrawn.

Discussion of Rejections Under 35 U.S.C. § 102

On a substantive basis, the Office Action rejected the independent claims (claims 1, 11, and 20) under 35 U.S.C. § 102 as allegedly anticipated by U.S. Patent 6,172,906 (hereafter the '906 patent). For at least the reasons set forth herein, Applicants respectfully request reconsideration of the rejection.

At the outset, Applicants note that the rejections are the same as the rejections set out in the previous Office Action, despite the amendments that Applicants made to the claims. Instead of altering the rejections, the Office Action merely referenced Applicants to the "Response to Arguments" section.

With regard to claim 1, claim 1 recites:

1. An integrated circuit component comprising:

logic capable of being configured to interface with a first portion of a system bus, wherein the first portion of the system bus comprises a first plurality of signal lines of the system bus, but not all of the signal lines of the system bus; and

logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus wherein the second portion of the signal bus comprises a second plurality of signal lines of the system bus, which are not a part of the first plurality of signal lines.

(*Emphasis added*). Applicants respectfully submit that claim 1 patently defines over the '906 patent for at least the reasons that the '906 patent fails to disclose the features emphasized above.

Notably, claim 1 is directed to "an integrated circuit component" (i.e., a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first portion of a system bus. Likewise, the second logic block is capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus. Simply stated, these features are not disclosed in the '906 patent.

To assist the Examiner in a better understanding of claim 1, consider the embodiment of Fig. 2 of the present application. The integrated circuit corresponds to reference numeral 210, while the companion integrated circuit corresponds to reference numeral 211. The first-recited logic element corresponds to split bus logic 214 of integrated circuit 210, while the second-recited logic element corresponds to split bus logic 215 of integrated circuit 210. As is illustrated in Fig. 2, and more particularly claimed in

claim 1, the first-recited logic element (e.g., split bus logic 214) is capable of being configured to interface with a first portion of the system bus 105. Likewise, the second-recited logic (e.g., split bus logic 215) is configured to communicate and receive information that is communicated over a second portion of a system bus and routed through the companion integrated circuit 211. Similarly, claim 1 also covers the embodiment of Fig. 5.

As previously noted by Applicants, the teachings applied by the Office Action from the '906 patent (disclosing two memory chips 670 and 672 of a memory bank 506) are simply inapplicable to the embodiments defined by claim 1. In this regard, the two memory chips 670 and 672 of the '906 patent are separate integrated circuits, and not a single integrated circuit as required by claim 1.

The Office Action responded to this previous argument by citing FIGs. 1 and 6. It appears that the Examiner is treating the reference number 600 (of the '906 patent) in FIG. 6a, for example, as denoting a chip. However, it instead denotes an entire memory system. The specification of the '906 patent confirms this (see col. 6, line 36 and col. 7, lines 47-52). Indeed, the Office Action (p. 15) states:

> Contrary to Applicants' argument, it is clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) each is disposed in a single integrated circuit chip.

This position reflects at least one fundamental misapplication of Estakhri to claim 1. As set forth above, reference number 600 (of Fig. 6a) denotes a "memory system" (col. 6, line 36), and not a single integrated circuit. Reference number 506 denotes a "memory bank" (col. 6, line 57), and not a single integrated circuit. Finally, by the Examiner's own admission that reference number 670 comprises a first integrated circuit and reference number 672

comprises a second integrated circuit, the two separate integrated circuits cannot properly/logically comprise a single integrated circuit chip, as expressly claimed by claim 1.

Rejection related to Amended Claim Language

The foregoing discussion is essentially a repeat of remarks from previous responses, as the Examiner has repeated the prior rejections (word for word). In fact, the only new discussion that the Examiner has made in response to Applicants' amendments is:

> Further, in anticipation that Applicants will address the issue of new matter, regarding the new limitations added to the claims, it is clear that each bus portion of the system bus of the '906 patent comprises a plurality of separate and different signal lines. See at least column 7, lines 1-9.

(Office Action, pp. 16-17). Applicant respectfully disagrees. In this regard, lines 1-9 of col. 7 of the '906 patent actually state:

> Memory bus 512 includes a flash bus 675 connected to a port 676 of memory I/O unit 652 for transmitting address, data, and command signals between flash memory chips 670, 672 and the memory I/O unit 652. Flash bus 675 includes 16 bit lines, 8 bit lines of which form a first bus 680 connected to a port 682 of I/O register 671 of the first flash memory chip, and another 8 bit lines of which form a second bus 684 connected to a port 686 of I/O register 673 of the second flash memory chip.

Even accepting this application of the '906 patent, the disclosure still fails to teach the claimed features. In this regard, assuming the sections 680 and 682 of the data bus comprises the claimed first and second plurality of signal lines, the memory chips 670 and 672 do not fulfill or provide the requisite features of claim 1. In this regard, claim 1 defines "***logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion***

integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus wherein the second portion of the signal bus comprises a second plurality of signal lines of the system bus, which are not a part of the first plurality of signal lines." No such comparable teaching or feature is disclosed in the'906 patent.

Simply stated, there is no teaching in the '906 patent of a single integrated circuit having logic for interfacing with a first portion of a system bus (the first portion being less than all of the system bus) and second logic for interfacing with a companion integrated circuit to receive information communicated over a second portion of the system bus. As claims 2-10 depend from claim 1, the substantive rejections of those claims should be withdrawn for at least the same reasons.

With regard to independent claim 11, claim 11 recites:

> 11. A system comprising:
> a plurality of companion integrated circuit components that collectively implement a logic function embodied in a single, conventional integrated circuit component, ***each companion integrated circuit component comprising***:
> a first logic interface for communicating with a remote component via ***a portion of a system bus, wherein the portion of the system bus comprises a plurality of signal of signal lines of the system bus, but not all of the signal lines of the system bus***;
> ***a second logic interface for communication with a companion logic interface of a remaining one of the plurality of the integrated circuit components over a separate bus***; and
> logic for controlling the selective communication of information received by the first logic interface via the portion of the system bus through the second logic interface to the companion integrated circuit.

(*Emphasis added*). Applicants respectfully submit that claim 11 defines over the '906 patent for at least the reasons that the '906 patent fails to teach those features emphasized above.

Like the rejection of claim 1, the Office Action cites memory chips 670 and 672 as comprising the claimed "integrated circuit." It then cites register 671 as comprising the claimed first logic interface. Then, the Office Action cites the same register 671 as comprising the claimed second logic interface. This rejection simply makes no sense, in the context of the claimed embodiments.

In this regard, the first logic interface is specifically claimed as "communicating with a remote component via a portion of a system bus." In contrast, the second logic interface is specifically claimed as being configured for "communication with companion logic interfaces of the remaining of the plurality of the integrated circuit components over a separate bus." This is not taught or disclosed in the '906 patent. In fact, the only input to the applied I/O register 671 is bit positions D[0:7] of the data bus 680. These bit positions couple to I/O register 671 at reference number 682. Significantly, the register 671 cannot comprise the claimed second logic interface, assuming that that register 671 comprises the first logic interface. Furthermore, the I/O registers 671 and 673 are disposed in separate integrated circuit chips, so these elements cannot be mixed and matched as applying to the first and second logic interfaces, as claim 11 requires that the first and second logic interfaces be in a single integrated circuit component.

For at least these reasons, the rejections of claim 11 should be withdrawn.

With regard to claim 20, independent claim 20 recites:

20. An integrated circuit component comprising:

a first set of conductive pins for channeling communications with a remote component via only a portion of a system bus, wherein the portion of the system bus comprises a plurality of signal of signal lines of the system bus, but not all of the signal lines of the system bus;

a second set of conductive pins for channeling communications with a companion integrated circuit component;

additional conductive pins for carrying additional control and communication signals;

wherein collectively, the conductive pins of the integrated circuit component do not directly accommodate all signals lines of the system bus, but rather directly accommodate fewer than all of the signal lines of the system bus.

The Office Action essentially copied the rejection of claim 1 and pasted it in the remarks section with respect the rejection of claim 20. In this regard, the Office Action referred to a "first logic interface" (see p. 11, line 9), even though no such element exists in claim 20.

In addition to the rejections copied from claim 1, the Office Action further concluded that "it is inherent that pins must be provided for connections between discrete chips or ICs." Finally, the Office Action alleged that "the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component." In essence, the rejection of claim 20 appears to take the position that the recited features are inherent in the structure recited in claims 1 or 11, and then relies on the rejections of those claims. In response, Applicants repeat and reallege the responsive remarks (above) with respect to the inapplicability of the '906 patent to claims 1 and 11. For the same reasons, the rejection of claim 20 should be withdrawn.

As the remaining claims depend from either claim 1, 11, or 20, all remaining claims 2-10, 12-19, and 21-24 patently define over the cited art.

DUTY OF DISCLOSURE

Applicants appreciate the Examiner's reminder regarding the duty of disclosure, and Applicant submits that this duty has been fully and properly discharged throughout the prosecution of this application. In response to the Examiner's remarks, however, Applicant wishes to make of record co-pending application serial number 10/630,260 (which the Examiner indicated that he believed to be a "related" application). That application is presently before the same Examiner (having just received a Decision on Appeal). In addition, the Examiner noted his belief that the present application and the applications of now-issued patents 7,099,994 and 7,103,826 are also inter-related.

The undersigned disagrees. The undersigned spoke with Examiner Dang by telephone on July 17, 2007, to better understand Examiner Dang's position on this. In this regard, the present application and the copending '260 application share some common figures and portions of the detailed description are common. Indeed, the undersigned drafted both applications, and explained to the Examiner (in the telephone discussion) that the applications were filed separately because they were believed to be patently distinct inventions. Indeed, the undersigned believes that, had the claims of the two applications been filed in a single application, the Patent Office would have issued a restriction requirement requiring them to be separated. Furthermore, the claims of the two separate cases embody subject matter that is unique to the specifications of each case (and not

described in the specification of the co-pending application). For this reason, the two applications have not claimed a formal relationship to each other.

The applications of the two now-issued patents noted above have even less relation to the subject matter of the present invention, as both of those patents are directed to RAID memory systems.

During the telephone discussion, the undersigned inquired of the Examiner whether the Applicant could combine the allowable claims from this application with the allowable claims of the co-pending '460 application, so that only one patent would issue (and therefore require only one set of maintenance fees). Examiner Dang said that such an action may result in a restriction requirement, and that he had not yet considered the claims from that perspective. Instead, the Examiner indicated that he considered the applications be related because they include certain drawing figures, and portions of the specification, in common.

Simply stated, the undersigned disagrees. Notwithstanding, the undersigned does wish to make of record the existence of the co-pending '260 pending application and notes that there is some subject matter overlap between these applications. Therefore, the Examiner should give the co-pending application a level of consideration that the Examiner believes to be appropriate to this application.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would

expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fees are believed to be due in connection with this amendment and response. If, however, any fees are deemed to be payable, you are hereby authorized to charge any such fees to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

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